

a first upper level of interconnect members formed over a semiconductor layer;

at least one lower level of interconnect members formed between the semiconductor layer

and the first upper level;

a first insulative material, having a relatively low dielectric constant, positioned to electrically isolate members of the first upper level from one another and extending to the lower level of interconnect members; and

a second insulative material, having a relatively high dielectric constant, positioned to electrically isolate members of the lower level from some of the electronic devices.

~~2. The structure of claim 1 wherein a portion of the second insulative material extends between an interconnect member of the lower level and an interconnect member of the upper level.~~

3. The structure of claim 1 wherein the second insulative material predominantly comprises silicon dioxide and the structure further includes a plurality of individual portions formed of the second insulative material, each portion extending between a member of the lower level and a member of the upper level and self-aligned with said member of the upper level.

4. The structure of claim 1 including at least a second upper level of interconnect members formed over the first upper level.

5. The structure of claim 1 further including a plurality of dielectric supports, formed of the same composition as the ~~lower~~<sup>second</sup> insulative material, each extending between one of the lower level interconnect members and one of the upper level interconnect members and providing physical support to sustain a spacial relationship between the lower level interconnect members and the upper level interconnect members.

6. The structure of claim 1 wherein members of the first level comprise Al, the first insulative material comprises hydrogen silsesquioxane and the second insulative material comprises silicon dioxide.

7. The structure of claim 1 further including a second upper level of interconnect members formed between the first upper level of interconnect members and the lower level of interconnect members wherein portions of the lower insulative material electrically isolate the second upper level of interconnect members from the lower level of interconnect members.

8. The structure of claim 1 further including:

a plurality of additional upper levels of interconnect members formed between the first upper level and the lower level;

4 a first layer formed of the first insulative material and positioned between the first upper  
5 level and a first of the additional levels; and

6 a second layer formed of the first insulative material and positioned between second and  
7 third ones of the additional levels.

1 9. The structure of claim 1 comprising second, third, fourth and fifth upper levels of  
2 interconnect members formed between the first upper level and the lower level.

1 10. The structure of claim 9 wherein the first, second, third, fourth and fifth upper levels  
2 are electrically isolated from one another by a continuous layer comprising the first insulative  
3 material.

1 11. The structure of claim 9 wherein the first insulative material is a single species of low  
2 k dielectric material and the second insulative material predominantly comprises silicon dioxide.

1 12. The structure of claim 9 wherein multiple layers each comprising the first insulative  
2 material electrically isolate the first, second, third, fourth and fifth upper levels from one another.

1 13. The structure of claim 1 further including a second upper level of interconnect  
2 members formed between the first level of interconnect members and the lower level of  
3 interconnect members wherein portions of the second insulative material extend to electrically  
4 isolate the second upper level of interconnect members from the lower level of interconnect  
5 members.

1 14. The structure of claim 12 wherein portions of the second insulative material extend  
2 between two or more of the upper levels.

1 15. The structure of Claim 1 further including:  
2 a first plurality of conductive portions extending at least between the upper level of interconnect  
3 and the lower level of interconnect; and  
4 a second plurality of conductive portions extending at least between the lower level of  
5 interconnect and some of the electronic devices.

1 16. The structure of claim 15 wherein the first plurality of conductive portions are  
2 integrally formed with members of the first upper level in a dual Damascene structure.

1 17. The structure of claim 15 wherein all of the members predominantly comprise Al.

1 18. The structure of claim 1 wherein the first insulative material extends from the first  
2 upper level to electrically isolate members of the lower level from one another.

1 19. The structure of claim 1 further including at least a second upper level of interconnect  
2 members formed over the first upper level of interconnect members with the first insulative  
3 material extending from the first upper level to electrically isolate members of the second upper  
4 level from one another.

1 20. A semiconductor structure comprising:  
2 a first upper level of interconnect members formed over a semiconductor layer;  
3 a lower level of interconnect members formed between the semiconductor layer and the  
4 first upper level; and

5 insulative material positioned to electrically isolate portions of the upper level of  
6 interconnect members from one another, portions of the upper level of interconnect members  
7 from portions of the lower level of interconnect members and portions of the lower level of  
8 interconnect members from one another,

9 said insulative material comprising a continuous layer extending from within regions  
10 between members of the upper level of interconnect to within regions between members of the  
11 lower level of interconnect, said continuous layer characterized by a dielectric constant less than  
12 3.9.

*regions for alignment*

1           21. The structure of claim 20 wherein the insulative material further includes portions  
2 extending between individual members of the upper level and individual members of the lower  
3 level, said portions formed of material having a dielectric constant greater than that of said  
4 continuous layer.

1 *Sub C1* 22. A method for forming a semiconductor structure, comprising:  
2 depositing a first insulative layer over a semiconductor layer;  
3 forming a lower level of interconnect members over the first insulative layer;  
4 depositing a second insulative layer between and over lower level interconnect members;  
5 forming an upper level of interconnect members over the second insulative layer  
6 removing portions of the second insulative layer positioned between interconnect  
7 members of the lower and upper levels; and  
8 forming a third insulative layer in regions from which the second insulative layer is  
9 removed.

1           23. The method of claim 22 wherein the second insulative layer comprises silicon  
2 dioxide and the third insulative layer has a relatively low dielectric constant relative to the second  
3 insulative layer.

1           24. The method of claim 22 further including the steps of:  
2 forming an additional level of interconnect members over the lower level of interconnect  
3 members;  
4 forming an additional insulative layer between and over members of said additional level;  
5 and  
6 replacing portions of the additional insulative layer with material having a low dielectric  
7 constant relative to silicon dioxide.

1           25. The method of claim 22 further including,  
2 forming a plurality of additional levels of interconnect members over the lower level of  
3 interconnect members;  
4 positioning additional insulative material between and over each of said additional levels  
5 of interconnect members; and  
6 replacing portions of the additional insulative material with material having a low  
7 dielectric constant relative to silicon dioxide.

1           26. The method of claim 22 wherein the step of forming an upper level of interconnect  
2 members over the second insulative layer comprises formation of a dual Damascene structure.

1 *Sub B1* 27. A method for fabricating an integrated circuit structure comprising:

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3 forming multiple levels of conductor lines over one another with some of the levels  
4 separated from one another by a layer of first insulative material;  
5 replacing portions of the first insulative material with a second insulative material having  
a dielectric constant lower than that of the first insulative material.

1 28. The method of claim 27 wherein the step of replacing portions of the first insulative  
2 material includes placing the second insulative material between conductor lines in at least one  
3 level.

1 29. The method of claim 28 wherein the step of replacing portions of the first insulative  
2 material comprises etching the first insulative material with one or more of the conductor lines  
3 masking other portions of the first insulative material thereby retaining said other portions in the  
4 integrated circuit structure.

1 30. The method of claim 29 wherein said other portions are self-aligned with masking  
2 conductor lines.

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1 31. A method for fabricating an integrated circuit having interconnect members formed  
2 over a semiconductor surface, comprising:

3 providing a first insulator material between interconnect members;  
4 replacing portions of the first insulator material with a dielectric material having a lower  
5 dielectric constant than the first insulator material.

1 32. The method of claim 31 wherein the first insulator material comprises silicon dioxide  
2 and the dielectric material is hydrogen silsesquioxane.

1 33. The method of claim 31 wherein the step of replacing the first insulator material  
2 comprises etching the first insulator material.